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Pulsed Direct Flame Deposition and Thermal Annealing of Transparent Amorphous Indium Zinc Oxide Films As Active Layers in Field Effect Transistors

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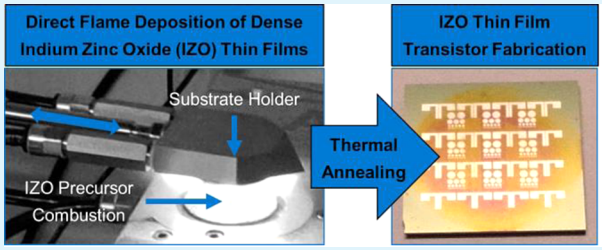
ABSTRACT: Indium−zinc oxide (IZO) films were deposited via flame spray pyrolysis (FSP) by pulsewise shooting a Si/SiO_2 substrate directly into the combustion area of the flame. Based on UV−vis measurements of thin-films deposited on glass substrates, the optimal deposition parameters with respect to low haze values and film thicknesses of around 100 nm were determined. Thermal annealing of the deposited films at temperatures between 300 and 700 °C was carried out and staggered bottom gate thin-film transistors (TFT) were fabricated.



The thin films were investigated by scanning electron microscopy, atomic force microscopy, X-ray diffraction, Fourier transformed infrared spectroscopy, and room-temperature photoluminescence measurements. The outcome of these investigations lead to two major requirements in order to implement a working TFT: (i) organic residues from the deposition process need to be removed and (ii) the net free charge carrier concentration has to be minimized by controlling the trap states in the semiconductor. The optimal annealing temperature was 300 °C as both requirements are fulfilled best in this case. This leads to field effect transistors with a low hysteresis, a saturation mobility of μ_{Sat} = 0.1 $cm^2/(V\ s)$, a threshold voltage of V_{th} = −18.9 V, and an I_{on}/I_{off} ratio on the order of 10^7. Depending on thermal treatment, the defect density changes significantly strongly influencing the transfer characteristics of the device.

KEYWORDS: *flame spray pyrolysis, direct deposition, field-effect transistor, amorphous metal oxides, indium−zinc oxide, thermal annealing*

INTRODUCTION

Amorphous oxide semiconductors (AOS) are a promising material class for active channel layers in thin film transistors, e.g. on flexible substrates.[1] A typical example is the ternary indium zinc oxide (IZO), where indium and zinc provide a high electron mobility within the conduction band even for a poor structural order. This effect is due to the spherical nature of the s orbitals that form the conduction band resulting in electrical conduction paths in the amorphous structure.[2,3] While the electrical performance of metal oxide based semiconductors is less sensitive to structural disorder than with other semiconductors, layers suitable for the incorporation in TFTs still need to fulfill certain requirements regarding their film morphology and their physical properties. Regarding the film morphology, the layers should form a smooth interface to the dielectric of the TFT structure, since the channel is formed there. A rough and porous interface increases the number of scattering events which hamper the charge carrier transport.[4] Furthermore, the film thickness needs to be in the range of the channel thickness. Due to the absence of blocking pn-junctions in TFTs based on metal oxides, the channel current between the source and drain electrodes is superimposed by a leakage current through the bulk of the material. A high film thickness therefore leads to a negative turn-on voltage V_{ON} for an n-type TFT because the layer has to be depleted first in order to decrease the current in the bulk of the semiconductor. The same effect can be observed if the free charge carrier concentration is high. The influence of the film thickness h and the free charge carrier concentration n_{free} on V_{ON} is given as[5,6]

$$V_{ON} \approx -\frac{q n_{free} h}{C_{ox}} \quad (1)$$

with q being the elementary charge and C_{ox} the capacitance of the gate dielectric. For the synthesis of an active layer, a large variety of processes can be applied including different sputtering techniques,[7−9] spray pyrolysis,[10−12] gas phase deposition,[13] sol−gel,[14] and solution based processes.[15,16] An interesting approach is a one-step direct deposition of thin films

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from a FSP process. FSP is a very versatile process for the synthesis of multicomponent materials as it is possible to mix several species on the liquid precursor level. In addition, metastable and amorphous phases are accessible due to the high temperature with subsequent cooling.[17] The film formation from FSP has been studied recently by Pratsinis et al. leading to a fundamental understanding of the underlying mechanisms.[17] Nevertheless, in most publications on FSP-based layer deposition, the deposition is carried out in a distinct region above the top of the flame front, where particle formation is already completed.[18−20] This leads to highly porous films with high surface areas and porosities, which can be very effectively used in applications such as gas sensors[21] or catalysts.[22] However, for active layers in TFTs dense films are required. For densification of the thin films flame annealing of the substrates is one opportunity. Tricoli et al. have shown a decrease in porosity from 98% to 62% of the volume-based layer porosity using this technique, which is still a much too high value for achieving acceptable active layer percolation in TFTs.[19]

To overcome the percolation issue, our approach is to directly deposit the thin film from the combustion zone of the flame, where droplets, nuclei and primary particles are present, but the number density of sintered aggregates, which lead to high porosities, is rather low. As the combustion zone exhibits very high temperatures in the range of 2200 K compact and well-sintered films are expected if the substrate is injected into the flame several times for a short period of time.[23] In order to avoid any damage or even breakage of the substrate a water cooled substrate holder is employed. In comparison to other processes, the advantages of pulsed direct flame deposition (PDFD) are the low post-treatment temperatures only needed for removal of precursor residuals rather than densification of the film. Additionally, due to the high precursor concentrations, high film growth rates in the order of 100 nm/s and therefore fast processing times for thin film fabrication are obtained. Furthermore, no cost-intensive (discontinuous) vacuum equipment is used as it is for sputtering techniques.

In this manuscript, we investigate the influence of post-treatment temperature on the thin film morphology, crystallinity, chemical purity and defect states. Furthermore, staggered bottom gate field effect transistors are fabricated. Finally, the transistor performance is discussed as a function of annealing temperatures, defect density and chemical purity.

EXPERIMENTAL SECTION

Precursor Formulation. As precursor for indium 0.08 mol/L indium(III) acetate (Alfa Aesar, 99.99%) and for zinc 0.113 mol/L zinc acetylacetonate hydrate (Sigma-Aldrich, 23−26% Zn) both dissolved in 2-Methoxyethanol (Sigma-Aldrich, 99.8%) is used. In order to increase solubility, 1 vol % acetic acid (Roth, 100% p.A.) is added to the zinc acetylacetonate solution and 1 vol % ethanolamine (Roth, 99% p.A.) is added to the indium acetate solution. Both solutions are ultrasonicated for 15 min separately. Afterward the solutions are mixed in a volumetric ratio of 60:40 (In:Zn) and heated in an oil bath at 70 °C for 15 min to obtain a stable solution mixture. The burner setup and the mode of operation have been described in detail elsewhere.[22] The applied FSP process parameters are shown in Table 1.

Pulsed Direct Deposition. In order to realize a more homogeneous radial temperature distribution and to prevent gas entrainment, a quartz glass tubing with 50 mm height and 40 mm diameter was placed around the burner. In consequence, the entrainment of surrounding gas toward the turbulent flame can be reduced up to that height. For the pulsed direct flame deposition a water cooled sample holder, which is mounted on a pneumatic-driven piston was constructed. The direction of the piston movement can be adjusted by a magnetic valve controlling the air support to the piston displacement chamber. By applying a certain upstream pressure the velocity of the piston movement is controllable. Therefore, with the aid of these installations the time for one back and forth stroke can be smoothly regulated within the millisecond range. The head of the substrate holder is tapered in order to reduce the disturbance upon entering the flame. As substrates for the thin film deposition we used boron-doped Si wafers with a 200 nm SiO_2 dielectric layer, which were mounted into the holder with the dielectric layer facing the flame. The whole setup consisting of the burner and the deposition device is schematically shown in Figure 1. The direct deposition device is shot in the flame in 70 mm height above the burner (HAB). In that case the deposition is taking place directly in the precursor combustion zone, as the total spray flame height is approximately 100 mm HAB. The time for one back and forth cycle is approximately 250 ms. This value was obtained by monitoring the piston movement with a high speed camera (not shown in this manuscript). All samples were prepared with 3 strokes into the flame. Both, the HAB and the necessary number of strokes were determined by prior investigations targeting sufficient substrate coverage, appropriate film thickness (around 100 nm) and transparency (see Results and Discussion section). Between subsequent strokes a delay time of 30 s is mandatory for cooling down the wafer. Too short interval times lead to unintentional heating of the substrate and may result in crack formation or even breaking of the whole substrate.

Table 1. Process Parameters for the IZO Deposition by Flame Spray Pyrolysis

precursor flow	9 mL/min
supporting O_2	3 L/min
fuel−CH_4	1.5 L/min
dispersion gas	9 L/min
sheath gas	1 L/min
nozzle pressure drop	2.5 bar

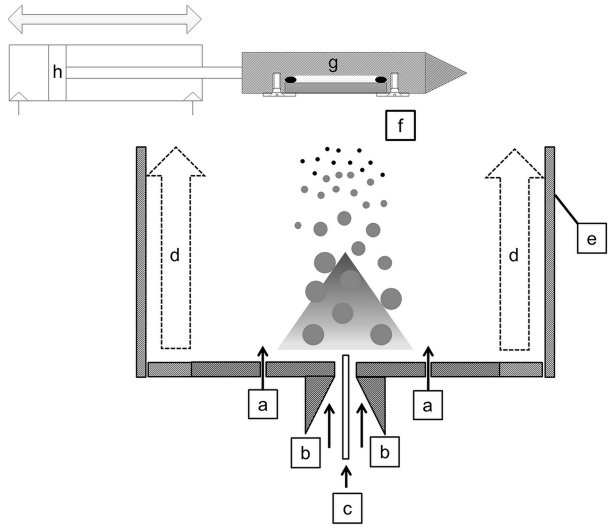

Figure 1. Schematic illustration of the deposition setup consisting of burner and direct deposition device: a = methane/oxygen annular gap outlet for the supporting flame, b = oxygen dispersion gas, c = capillary for precursor supply, d = sheath gas flow, e = 50 mm height quartz glas tubing, f = Si/SiO_2 substrate, g = substrate holder, h = pneumatic piston.

Thermal Annealing. For thermal annealing all substrates were heated under ambient atmosphere for 1 h at temperatures of 300, 400, 500, 600, or 700 °C. Afterward the substrates were cooled down in the

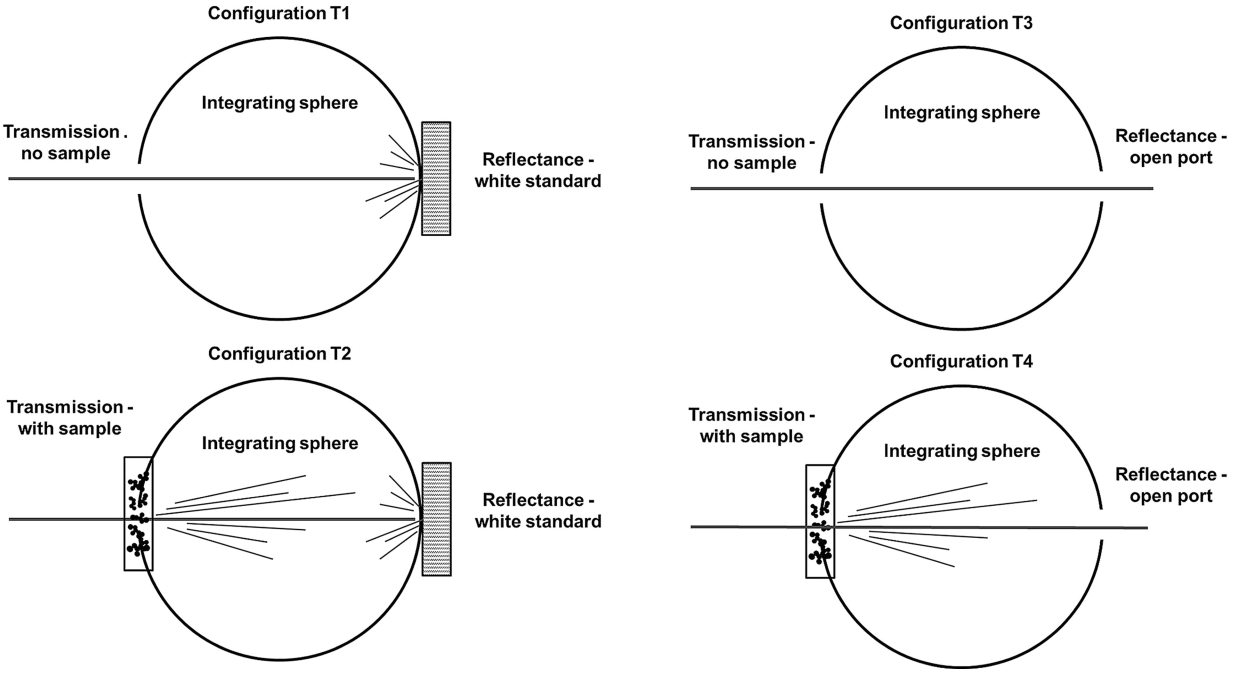

Figure 2. Four spectrophotometer setups for haze measurements according to Active Standard ASTM D1003.

furnace to ambient temperature by natural convection. The influence of thermal annealing on film morphology, crystallinity, chemical purity, defect states, and transistor performance is investigated.

Analytics. For the determination of film thickness, wetting between dielectric and deposited active layer, morphology, and thin film structure, scanning electron microscopy (SEM) (Ultra FE-SEM Gemini Ultra 55, Carl Zeiss, Jena, Germany) is applied with an acceleration voltage of 10 keV and in-lens detection with 30 μm aperture for high-resolution imaging. In addition, atomic force microscopy (AFM) with a JPK Nanowizard II BioAFM system (JPK Instruments, Berlin, Germany) on a 10 μm × 10 μm area in tapping-mode is utilized. As cantilever we used a NSC 15 from MikroMasch. The structure of the thin films is analyzed by X-ray diffraction (X'Pert PRO MRD, Panalytical, Almelo, Netherlands) in grazing incidence (GI-XRD) geometry with an incidence angle of 1°. As already mentioned before, the deposition takes place directly in the precursor combustion zone where unconverted solvent or precursor residues may be incorporated in the film leading to insulation effects in the device. Due to that, grazing incidence Fourier transformed infrared spectroscopy (GI-FTIR) with a Bruker EQUINOX 55 equipped with a BRUKER IRscope II (BRUKER, Billerica, United States) is carried out to identify organic residues in the film. The spectra were taken between 4000 and 1400 cm^{-1} wavenumbers with a resolution of 1.285 cm^{-1}. For characterization of the defect luminescence, room temperature photoluminescence measurements (FluoroLog, Horiba Ltd., Kyoto, Japan) of the thin films were carried out. The excitation wavelength is 325 nm and the emission spectrum was detected between 200 and 800 nm with a resolution of 1 nm. All mentioned measurement techniques in the later sections were carried out for the *as deposited* film and the different annealing temperatures. Furthermore, films without any thermal treatment were deposited with different stroke numbers on 1 mm glass substrates in order to investigate the haze of the film. This was done by UV/vis diffuse-reflectance spectroscopy with a PerkinElmer Lambda 15 spectrophotometer, equipped with an integrating sphere. The spectrum is gathered between 380 and 780 nm (visible range) with a resolution of 1 nm. Therefore, four different transmissions scans with configurations T1−T4 of the diffuse reflectance UV/vis spectrophotometer need to be carried out according to Figure 2.

The evaluation of the four gathered spectra is done according to the Active Standard ASTM D1003-11e1 standard procedure for the calculation of the haze value. By integrating the area under each transmission spectra, the integral transmittances T_1, T_2, T_3, and T_4 for each configuration are calculated. The haze value can then be calculated according to eq 2

$$\text{haze}[\%] = \left[\left(\frac{T_4}{T_2}\right) - \left(\frac{T_3}{T_1}\right)\right] \times 100\% \quad (2)$$

In order to evaluate the potential of the deposited layers for application as active layer in TFTs, staggered bottom gate TFTs were fabricated. The p^+-silicon substrate served as gate electrode while the 200 nm SiO_2 was used as the gate dielectric. The structures were completed by the evaporation of aluminum through a shadow mask to form the source and drain contacts on top of the IZO layer. The source and drain electrodes had a thickness of 100 nm and defined a channel region with a width W of 2000 μm and a length L of 80 μm. The electrical characterization of the devices was carried out with two 2636 dual-channel source meter instruments from Keithley Instruments. All measurements were made in a glovebox under nitrogen atmosphere and the exclusion of light.

RESULTS AND DISCUSSION

Optical Haze Measurements. In Figure 3 the results of optical haze measurements for different numbers of strokes compared to a pure glass substrate are shown.

As expected, the deposition of the thin film increases the haze with increasing number of strokes compared to a blank glass substrate. For 3 to 5 stroke cycles the haze stays below 4% in the whole visible range. The film thickness in these cases is between 80 and 180 nm. For 10 strokes the film has a thickness of around 400 nm, which is in the range of the incident wavelength and therefore scattering effects significantly increase the haze of the film. As a major goal is to achieve a high transparency and a low haze value, the thin films prepared with 3−5 strokes are most suitable. Moreover, the film should be as thin as possible while the substrate dielectric layer should be completely wetted and covered in order to facilitate the channel formation in a TFT. Previously analyzed SEM pictures of thin films deposited with one or two strokes showed no sufficient substrate coverage (not shown in this manuscript). Based on

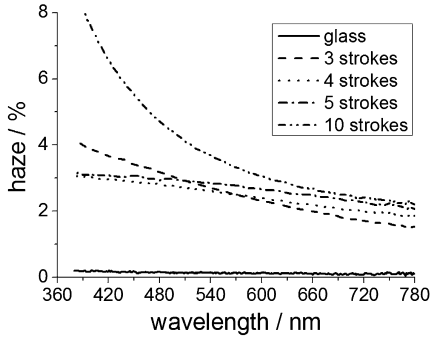

Figure 3. Haze measurements in the visible range for different stroke numbers.

the results of the haze study, completely covered, highly transparent, and approx. 100 nm thin films were fabricated for the thermal annealing study with the following deposition parameters: a residence time of 250 ms in the flame, three stroke cycles with 30 s delay time in between, and a deposition height of 70 mm.

Influence of Thermal Annealing on Film Morphology. In order to determine the film thickness and the homogeneity of the wetting of the IZO thin film to the dielectric SiO_2 layer, IZO coated substrates were cleaved to further analyze them by SEM in side view. In Figure 4 cross sections of the as-deposited

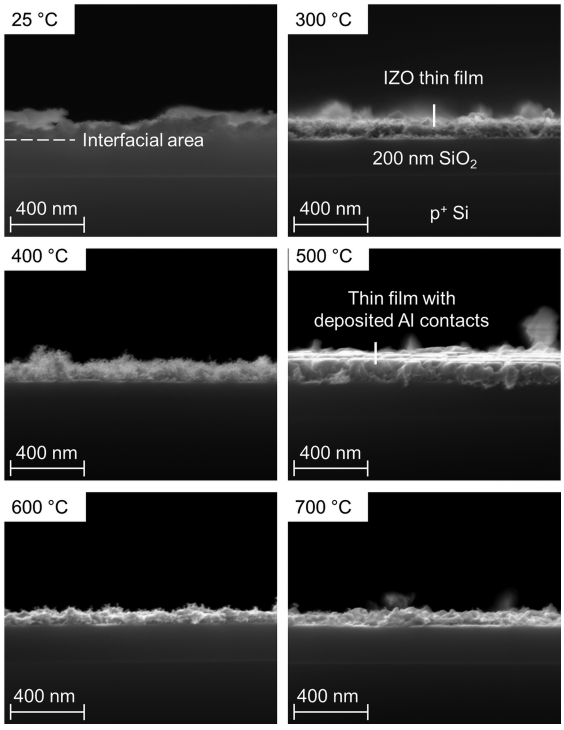

Figure 4. SEM micrographs of cleaved Si/SiO_2 wafer substrates. The wetting of the IZO thin film to the dielectric SiO_2 layer is homogeneous and no cracks were found over the whole sample area.

and post-treated substrates are shown. The mean film thickness and its standard deviation was determined by measuring the distance of five randomly chosen points orthogonal to the surface of the dielectric layer to the top of the IZO thin film. The thickness varies between 84 and 135 nm. The interfacial area between the dielectric SiO_2 and the IZO active layer shows a very uniform and homogeneous crack-free wetting all over the sample which is not influenced by variation of the annealing temperature.

Furthermore, in Figure 5 SEM micrographs in top view of the deposited and annealed IZO thin films are depicted. All

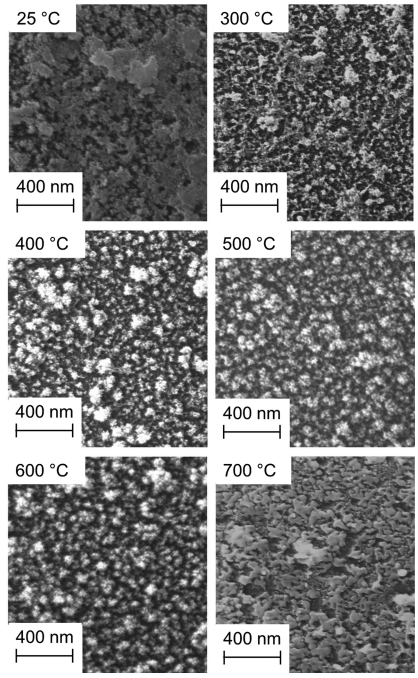

Figure 5. SEM micrographs (top view) of the deposited and annealed IZO thin films. Two morphological changes can be seen from as deposited (25 °C) to 300 and 600 to 700 °C annealing temperatures.

images show a rather rough surface with interconnected, partially sintered structures. For 25 °C the surface of the film shows more planar areas, which is due to the deposition of precursor droplets in the interspace between the IZO thin film. Applying a temperature of 300 °C may lead to further precursor conversion forming "cauliflower-like" structures, which is comparable with the results from Tricoli et al.[19] This film morphology is stable up to a temperature of 600 °C. By further increasing the temperature to 700 °C, coalescence of grains occurred leading to a more connected structure compared to the lower temperatures. The results from the SEM top view regarding the change in surface morphology from 25 to 300 °C can be also observed by AFM. Figure 6 shows the AFM micrographs of an as-deposited (top image) and 300 °C thermal annealed thin film (bottom image). The as-deposited film shows more agglomerated and interconnected "island" structures, while the thermally treated film appears more homogeneous. However, the surface of the IZO thin film appears relatively inhomogeneous as there are height differences in the order of the film thickness. Nonetheless, as the electric channel for charge carrier transport develops at the interface SiO_2/IZO the device characteristics are negligible influenced. Furthermore, the roughness of all temperature-treated samples was analyzed leading to roughness R_a values between 14 and 25 nm with no clear trend for the different annealing temperatures.

Influence of Thermal Treatment on Crystallinity. As already mentioned in the introduction, an amorphous film structure may be favored for homogeneity of film formation.

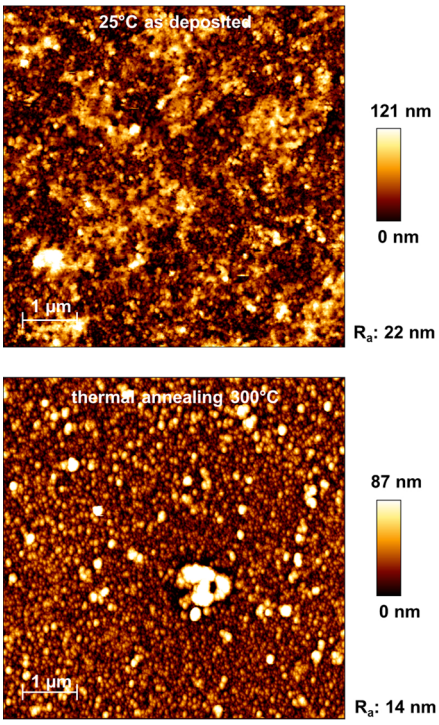

Figure 6. AFM topology for untreated and thermally treated thin films. Temperature treatment leads to a more grain-like structure of the film.

Therefore, the structure of the annealed thin films was investigated by GI-XRD (see Figure 7). Both, the as-deposited

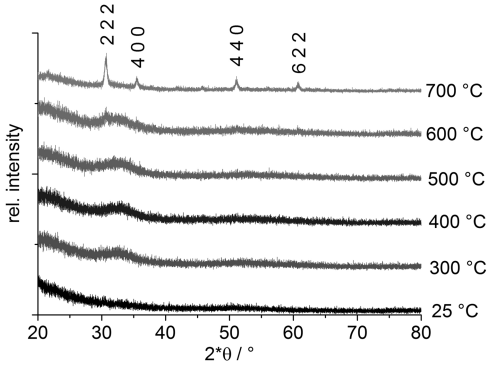

Figure 7. GI-XRD measurements as a function of annealing temperature. At 700 °C cubic In_2O_3 crystallizes in the thin film.

and the annealed thin films showed an amorphous or mostly nanocrystalline microstructure up to a temperature of 600 °C. At 700 °C GI-XRD revealed that cubic In_2O_3 crystals are formed. This observation leads us to the assumption that the increased temperature favors solid-state diffusion processes, subsequent oxygen diffusion and consequently rearrangement of the atoms in the thin film.

Influence of Thermal Treatment on Chemical Purity. Due to their insulating character, organics at the surface or incorporated in the thin film negatively affect the electron transport. Thermal annealing is therefore mandatory in order to remove any organic residues. In flame spray pyrolysis the droplet size, spatial droplet distribution, droplet velocity, and temperature are radially and axially distributed.[24] Consequently there are droplets, nuclei and primary particles coexisting in the direct deposition area. Therefore, it is obvious that unreacted precursor and solvent may be incorporated into the film. This can clearly be shown by the GI-FTIR measurements (see Figure 8).

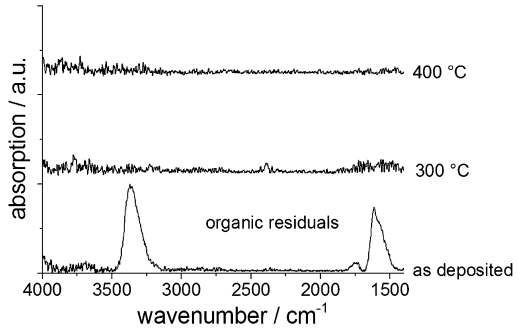

Figure 8. GI-FTIR measurements as a function of annealing temperature. The as deposited film shows C═O and O−H stretching modes, which can be removed by temperature treatment.

The as deposited thin film shows two IR absorption bands at maximum wavenumbers of 1617 and 3368 cm^{-1}, which can be assigned to C═O and O−H stretching modes, respectively. Both may arise either from the solvent 2-methoxyethanol or the acetylacetonate and their decomposition byproducts due to an incomplete combustion upon deposition on the substrates. In contrast to that, the spectra of the annealed thin films show no absorption at all wavenumbers.

Influence of Thermal Annealing on Luminescence Emission. To obtain an integral view on the nature and density of defects, room-temperature PL measurements were carried out on the thin films (see Figure 9a). These measurements are very closely connected to the device performance as defects in the active layer might act as donators or traps for charge carriers and are thus directly influencing the device performance. As amorphous materials do not have a crystalline long-range order, defects in this material class may arise from nonsaturated atomic bonds rather than from discrete point defects known from crystalline materials. For the as-deposited sample the defects in the thin film occur due to the very fast thermophoretic deposition rate. In a comparable setup carried out in the work of Mädler et al. thermophoretic deposition rates for rather low temperature gradients around 500 °C were calculated to be around 0.1 to 1 μm/s.[21] These values fit very well to our observed film growth rates. In contrast to that, the crystallization time to attain equilibrium in IZO systems in our composition range was reported to be several days for temperatures above 1300 °C.[25] Consequently the direct deposition process is several orders of magnitude faster and may lead to a high number of unsaturated atomic bonds. This can be clearly seen from the broad PL intensity distribution of the as deposited sample in Figure 9a. We assign this broad emission peak between 370 and 600 nm to electron transitions to deep defect states. As the wavelength range of luminescence emission is very broad, we assume that the as deposited film exhibits a mixture of several types of radiatively recombing states, e.g. organic species from the deposition process and/or the previously mentioned unsaturated atomic bonds. By exposing the thin films to air and higher temperatures, oxygen might recombine with oxygen vacancies and thereby saturate the film by diffusion processes or the metal ions in the film themselves might rearrange and therefore lower the defect

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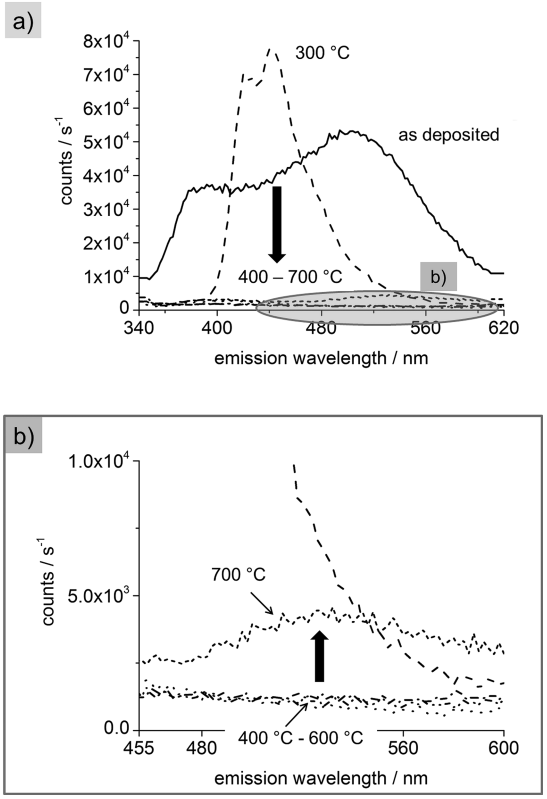

Figure 9. (a) Room temperature photoluminescence spectra for different annealing temperatures. The defect density decreases with increasing temperature and is almost completely removed between 400 and 600 °C. (b) At 700 °C, In_2O_3 recrystallization leads to a slight increase in defect density.

density. The latter thermal activated diffusion processes have also been reported in literature at 300 °C, where rearrangement processes of intermetallic In−In and Zn−Zn bonds toward metal oxide In−O and Zn−O bonds are observed.[7] This trend is clearly evident for the samples treated at 300 °C for 1 h: The wavelength range of luminescence emission is between 400 and 530 nm and therefore narrower compared to the as deposited sample. This indicates the saturation or elimination of defect states and/or the removal of organic species. Nevertheless, the overall intensity in this wavelength range increased, which cannot be completely explained at the moment. A reason might be the change in morphology, which leads to microstructural changes in the atomic short-range order of the thin film resulting in a different surface modification. For 400−600 °C the emission luminescence intensity vanished indicating a low defect concentration for the applied excitation wavelength. For 700 °C (see Figure 9b) the defect luminescence slightly increases again compared to the samples annealed between 400 and 600 °C but is significantly lower than for the as deposited and 300 °C treated samples.

A possible reason for this observation is the crystallization of In_2O_3 nanocrystals (Figure 6), which was observed in the GI-XRD measurements. Oxygen for the formation of In_2O_3 can be supplied either by the surrounding air environment or by diffusion of mobile oxygen from the thin film to indium atoms.

Transfer Characteristics As a Function of Annealing Temperature. In Figure 10, the transfer characteristic for TFTs are shown as a function of different annealing temperatures. For the as deposited sample the drain current

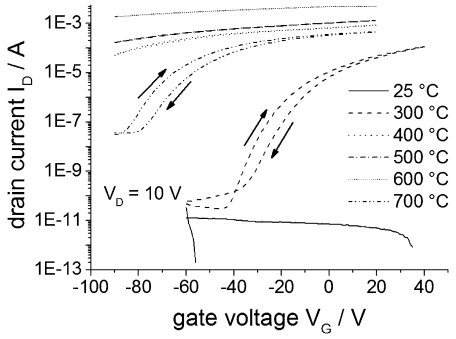

Figure 10. Comparison of TFTs thermally treated at different temperatures. Transfer characteristics were measured for a constant drain voltage of 10 V.

is of around 10^{-11} A and does not increase with increasing gate voltage. For 300 °C, typical transfer characteristics are obtained as with increasing gate voltage the drain current increases significantly as well. For 400−600 °C the drain current is almost independent of the gate voltage and we refer to this as quasi-metallic behavior, as the absolute measured drain current values reach high values up to 10^{-3} A. For 700 °C, we again get a working field effect transistor.

For a TFT to have a turn on voltage close to 0 V and a low off current, the free charge carrier concentration should be small. The free charge carrier concentration for a trap free semiconductor equals the doping concentration, assuming that all dopants are ionized. If trap states in the band gap are present, however, charge carriers can be localized in such states. Therefore, the free charge carrier concentration will be reduced depending on the concentration of trap states.[5]

In photoluminescence measurements an excess of charge carriers is created by optical excitation and the radiative recombination processes are monitored. A high defect luminescence from deep states within the band gap can be correlated to a high trap state density which can compensate dopants, leading to a low free charge carrier concentration.

Comparing the transfer characteristics with the luminescence emission spectra we can clearly see a connection to the defect states. For 25 °C the high defect density does not play a role as the thin film is highly contaminated by organic groups from unconverted precursor (see FTIR measurements). The organics act as insulating barrier between IZO regions resulting in a high resistance and no semiconducting behavior in the active layer. For 300 °C the free charge carrier concentration is reduced via electron trapping in deep states. Injected charge carriers can be accumulated by applying a gate voltage and form a conductive channel at the interface between the gate-dielectric and the active layer, which results in typical transfer characteristics for a TFT with a threshold voltage of V_{th} = −18.9 V, saturation mobility μ_{Sat} = 1.4 × 10^{-1} $cm^2/(V\ s)$ and, depending on the applied drain voltage, an I_{on}/I_{off} ratio in the order of 10^7. For samples annealed at 400−600 °C, the defect states have almost vanished according to the PL emission (see Figure 9). This leads to a low trap density and thus most charge carriers may contribute to the electron transport resulting in the behavior of a degenerated semiconductor. This can be clearly seen in Figure 10 where almost no modulation of the drain current with the applied gate-voltage can be observed. Nevertheless, the measured drain current is very high, around 10^{-4}−10^{-3} A, indicating an excess of free charge carriers. For 700 °C, defect states are reinduced by the phase trans-

formation, but their PL emission intensity is 1 order of magnitude lower than for 300 °C. This results in characteristic TFT behavior but with worse TFT specific values compared to the 300 °C transistor as the free charge carrier concentration seems to be higher as indicated by a threshold voltage of V_{th} = −75.3 V. The saturation mobility μ_{Sat} was extracted to be 0.43 $cm^2/(V\ s)$ and depending on the applied drain voltage an I_{on}/I_{off} ratio in the order of 10^4. Both working TFTs exhibit a small hysteresis effect and the onset voltage is shifted towards negative gate voltages namely around −20 V for 300 °C and around −80 V for 700 °C annealing temperature.

CONCLUSION

We were able to deposit amorphous IZO layers directly from the flame by a pulsed deposition device onto Si/SiO_2 substrates. The thin films exhibited excellent transparency in the visible range. After deposition the films are exposed to temperatures between 300 and 700 °C in ambient air atmosphere. SEM and AFM measurements showed that the morphology of the thin films is dense and homogeneous. The boundary layer between SiO_2 gate dielectric and the thin film exhibits a very uniform wetting, which should support a homogeneous development of the conducting electron channel in a TFT device. Furthermore, the thin films are amorphous up to an annealing temperature of 700 °C. At this temperature GI-XRD measurements show the crystallization of cubic In_2O_3 crystals. In order to reduce the charge carrier concentration and to get a working TFT the doping concentration should be low or compensated by trap states. Thermal annealing at 300 °C showed the best TFT performance as the defect density is still high and insulating organic impurities were completely removed from the thin film.

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Notes

The authors declare no competing financial interest.

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